<u>Computer Organisation (Exam No. 3)</u>

ACS Diploma of Information Technology
Examiner's Report June 2009

Computer Organisation

Computer Organisation had 14 students appearing in the June 2009 exam. All except one passed the exam. The exam format was similar to the previous exams and there were a total of ten questions covering areas such as computer's organization, its memory mechanisms, the speed of the CPU and storage. However, similar to the past few runs of the exam, specific competencies were not applied, as the structure of the exam was based on the previous run of the exam. However, there were at least a couple of students who seem to apply past exam answers to questions that had been slightly changed. In such cases, students received minimal marks corresponding only to their methods demonstrated and not towards the final answer, which was incorrect. Students are therefore encouraged NOT to learn the answers here by-heart, but understand the concepts and methods behind the answers. Some of the specific questions and the way in which they should have been attempted are described below (students should note again *that they are expected to add more material to their answers than is shown here that demonstrates their own reading and understanding on the subject material).*

Question One

What is the difference between a computer's storage mechanism versus its computing mechanism? Explain with examples. **(10 marks)**

The answer is meant to provide, in detail, the difference between storage and computing. Thus, there is a need to explain the "main" memory that is permanently on the disk as well as the temporary memory that is understood as the computer memory. This main memory is also called RAM (Random Access Memory), and it is the binary electronic space where both data and program are stored during computations carried out by the computer. The virtual storage/memory is a part of the auxiliary storage of the computer. This virtual storage is an extension of main memory which is addressable main memory by the computer. The size of the virtual storage is limited by the mechanism by which the computer addresses the memory locations as also by the amount of auxiliary storage available in the computer. This is so because, through virtual storage, running programs can address memory locations which do not currently reside in the main memory – but will be fetched by the operating system.
Multiprogramming implies that the computer's processor is running more than one program concurrently. A computer capable of multiprogramming will have its central processing unit (CPU) handling many programs simultaneously. However, multiprogramming will be successful not only with the computer's capability but also with the virtual memory capacity of the computer.

Question Two

Convert the decimal number 14 into hexadecimal number and binary numbers. You must show the working process of this conversion. **(10 marks)**

Hexadecimals are able to represent the numbers 0 to 15; this is done by using the digits 0 to 9 followed by characters A to F.

Thus, a Decimal 14 (14 base10) = 14;
14 should be divided by 16 to arrive at the numbers. In this case, however, 10 is equal to A, 11 is B and 12 is C, 13 is D and 14 is E.
Therefore the answer will be ‘E’$_{base}$16.

And a Decimal 14_{10} = Binary – (1 1 1 0)$_{base}$2

Question Three
Simplify the following logic expression:
E= AB(B+C)’+ (A’+B)’ + C(A’ + B’)’ **(10 marks)**

E = ABB’C’ + AB’ + CAB
E = AB’ + ABC

Students should note that additional steps can and should be shown.

Question Four

(a) Consider a microprocessor, with a 32-bit external data bus, driven by a 1200-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals eight input clock cycles. What is the maximum data transfer rate that this microprocessor can sustain? Your answer *must* be supported by all the steps you use in arriving at the answer. **(10 marks)**

The Maximum data transfer rate for a microprocessor is given by its = bus cycle speed x width of a data bus (in bits)

For a, 1200 MHz clock, the Bus cycle speed is:
1200 / 8 = 150 million cycles per second

For a 32-bit external data bus the
Maximum data transfer rate = 150 x 32 = 4,800 million bits per second
= 4.8 Gbps

Question Five
Show how computers carry out the operation (11_{10}-21_{10}) using 2’s complement, assuming 8 bits are used to represent each decimal number (11_{10} and 21_{10} indicate decimal numbers of 11 and 21 respectively). You must show how each number is represented, the working process and the interpretation of the result. **(10 marks)**

- 11base10 in 2’s compliment is = 00001011 +
- 21base10 in 2’s compliment is = (+21base10) 00010101;
  - Bitwise compliment = 11101010
  - + 1 = 11101011

11110110 $_2$

Since the above is the result based on 2’s compliment, which can be shown as:
10001010

Question Six

If a processor's address width is 32 bits, how many addressable locations does the processor have? Ensure your answer is fully justified (*Note: simply writing the answer will not attract full marks)* **(10 marks)**

In many system the addressable unit is the word; however, in other systems, the addressing can be achieved at byte level too. In this case, the address width is 32 bits. This means each memory location can store 32 bits of data and if we assume that the memory is 128 MB, the addressable locations are:

$(128 \times 2^{32}) / 4 =$
$(2^{7} \times 2^{32}) / 2^{2} = 2^{37}$
Addressable locations

Question Seven
A computer has a cache, main memory, and a disk used for virtual memory. If a word is in the cache, 32 nanoseconds are required to access it. If it is in main memory but not in the cache, 240 nanoseconds are first needed to load it into the cache, and then the reference is started again. If the word is not in main memory, 400 nanoseconds are needed to transfer it to the cache and the reference is started again. If the cache hit ratio is 50% and the main memory hit ratio is 40%, what is the average access time? **(10 marks)**

Average access time of cache = 32 ns
Time needed to load into cache = 240 ns
Time needed to load in cache and reference start again = 400 ns
Cache hit ratio = 50%
Main memory hit ratio = 40%
Average access time = (0.5 x 32) + 0.40 x (240 + 32) + (400 + 32)
= 16 + 0.4 + 272 + 432

= 720 ns

Question Eight
(i) What are the main stages of an instruction cycle? (ii) Explain how instruction pipelining can improve computer efficiency. (**10 marks)**

There are 6 stages in an instruction cycle:
Fetching the required instructions from the memory
Decoding and interpreting the instructions
Execution of the decoded instructions by the Arithmetic Logic Unit
Transfer of control instructions
Perform arithmetic / logical functions
Load and store the instruction as results in the memory

Instruction pipelining can be considered as a multiple assembly line, wherein similar processes can be worked out simultaneously. Thus, instruction pipelining is an introduction execution method in which instructions are divided in number of stages and multiple instructions at different stages are executed at the same time. Furthermore, while one instruction is being executed, another could be simultaneously loaded into memory which, otherwise, wouldn't be accessed. Thus in instruction pipelining, different stages of instructions are executed at the same time by making use of different resources of the CPU – this results in efficient processing by the computer.

Question Nine

(i) Explain how to calculate the storage requirement of a bit-mapped graphics/image. (ii) What is the storage requirement of a bit mapped image of 1000 x 800 pixels with 24 bits per pixel? (**10 marks**)

(W x H x D) / 8 (bytes)

The above will be the way in which one can calculate the storage requirements of a bit-mapped image - assuming that a bit mapped graphic has a height of H pixels, width of W pixels and depth D bits per pixel, and amount of storage is given in bytes.

(1000 x 1200 x 24) bits / 8 = 2,800,000 bytes.

Question Ten

"DRAMs are normally cheaper and larger in storage size than SRAMs. So SRAMs are not used in most computers." (i) Is this statement correct? (ii) Justify your answer.

(10 marks)

The statement is incorrect.

This is so because even though Dynamic Random Access Memory (DRAM) are cheaper and larger in size than Static Random Access Memory (SRAMS), they are slower than SRAMs. Hence SRAMS are used for critical parts of computers where speed is essential, like a cache; however, DRAMs are used in main memory.